AMENDMENTS TO THE CLAIMS

1. (currently amended) A method of transferring stored digital parallel data of multiple bits of data stored in a first data register from a transmitter to a receiver over a hard wired conductor comprising the steps of:

synchronously converting said stored digital data to a serial analog data signal in said transmitter;

transmitting said serial analog signal asynchronously over said hard wired conductor to said receiver; and

restoring said asynchronous serial analog signal to synchronous digital parallel data in said receiver corresponding to the data stored in said first data register in said transmitter, including detecting both edges of the data in said asynchronous serial analog signal for conversion to parallel data bits and using a phase rotator operating under the control of a phase lock loop to convert said asynchronous signal to said synchronous digital parallel data in conjunction with said edge detection.

2. (Original) The invention as defined in claim 1 wherein the digital parallel data is read out of said first data register to at least one single bit latch.

3. (Previously presented) The invention as defined in claim 2 wherein the data is read out from said first register in said transmitter two bits at a time, each data bit to first and second single data bit latches, and from each first and second single bit data latch to a third single bit data latch, clocking additional two data bits to be

subsequently written to said first and second one bit latches and to said third single bit data latch until all bits of the data have been read from the first register.

4. (currently amended) The invention as defined in claim 3 wherein the bits from the third single bit ~~register~~latch are converted to a single analog serial signal of the data.

5. (Original) The invention as defined in claim 1 wherein the data in said first register is comprised of either eight or ten bits.

6. (Original) The invention as defined in claim 1 wherein a clocking signal is used to convert said analog serial signal to a digital signal.

7. (currently amended) The invention as defined in claim 3 wherein said analog signal is converted in said receiver to two one-bit signals and delivered to a shift ~~latch~~register and then stored in a second data ~~latch~~register.

8. (currently amended) The invention as defined in claim 7 wherein said bits in the shift ~~latch~~register are delivered synchronously from said shift ~~latch~~register to said second data ~~latch~~register.

9. (Original) The invention as defined in claim 1 wherein said edges are derived from multiple samples.

10. (Original) The invention as defined in claim 9 wherein said multiple samples are used to determine the approximate center of said resulting data bit.

11. (currently amended) A structure for transferring stored digital parallel data of multiple bits of data stored in a first data register, comprising a transmitter and a receiver connected by a hard wired conductor;

circuitry to synchronously convert said stored digital data to a serial analog data signal in said transmitter;

circuitry to transmit said serial analog signal asynchronously over said hard wired conductor to said receiver; and

circuitry to restore said asynchronous serial analog signal to synchronous digital parallel data in said receiver corresponding to the data stored in said first data register in said transmitter, including detecting both edges of the data in said asynchronous serial analog signal for conversion to parallel data bits, said circuitry to restore said asynchronous signal to said synchronous digital data, including a phase rotator operating under the control of a phase lock loop to act in conjunction with the circuitry to detect both edges.

12. (Original) The invention as defined in claim 11 including at least one single bit latch and circuitry to read the digital parallel data out of said first data register to said at least one single bit latch.

13. (Previously presented) The invention as defined in claim 12 including first, second and third single data bit latches, and wherein the data is read out from said first register in said transmitter two bits at a time, each data bit to either said first or second single data bit latches, and then from each first and second single bit data latch to said third single bit data latch, clocking to clock additional two data bits to be subsequently written to said first and second one bit latches and to said third single bit data latch until all bits of the data have been read from the first register.

14. (Previously presented) The invention as defined in claim 13 including circuitry to convert the bits from the third single bit latch into a single analog serial signal of the data.

15. (Original) The invention as defined in claim 11 wherein the data in said first register is comprised of either eight or ten bits.

16. (Original) The invention as defined in claim 11 including a clocking signal to convert said analog serial signal to a digital signal.

17. (currently amended) The invention as defined in claim 11 including a second data bit ~~latch~~register and circuitry in said receiver to convert said analog signal to two one-bit signals delivered to a shift ~~latch~~register, and store the converted bits in said second data ~~latch~~register.

18. (currently amended) The invention as defined in claim 17 wherein said bits in the shift register are delivered synchronously from said shift register to said second data ~~latch~~register.

19. (Original) The invention as defined in claim 11 including circuitry to derive said edges from multiple samples.

20. (Original) The invention as defined in claim 19 wherein said circuitry to derive said edges from said multiple samples determines the approximate center of said resulting data bit.